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PATENT DATE

APPLICATION NO. CONT/PRIOR CLASS SUBCLASS ART UNIT EXAMINER 438 25 / 09/876290 2812 <del>28</del>7 F Man War 686

Yoshiyuki Yanagisawa Toshiharu Yanagida Masashi Enda Yuichi Takai

35.75 A

Assembly jig and manufacturing method of multilayer semiconductor device  $\dot{}$ 

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PTO-2040 12/99

		ISSUING C	LASSIFICATION			
ORIGINAL			CROSS REFERENCE(S)			
CLASS SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)			
INTERNATIONAL	_ CLASSIFICATION					
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	DRAWINGS	ì	CLAIMS ALLOWED		
Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.	
	1		NOTICE OF ALL	OWANCE MAILED	
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				5, Sections 122, 181 and 368.	
	(Assistant (Primary E (Legal Instrume	(Assistant Examiner)  (Primary Examiner)  (Legal Instruments Examiner)	(Primary Examiner) (Date)  (Primary Examiner) (Date)  (Legal Instruments Examiner) (Date)	(Assistant Examiner) (Date)  ISSI  Amount Due  (Primary Examiner) (Date)  ISSUE BAT  (Legal Instruments Examiner) (Date)  stricted. Unauthorized disclosure may be prohibited by the United States Code Title 3strack Office is restricted to authorized employees and contractors only.	

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